

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bratin Saha

Art Unit : Unknown

Serial No. :

Examiner : Unknown

Filed : March 9, 2004

Title : SYNCHRONIZATION OF PARALLEL PROCESSES

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant submits the references listed on the attached form PTO-1449.

This statement is being filed with the application. Accordingly, only copies of foreign patent documents and non-patent literature are enclosed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 03/09/2004


William E. Hunter
Reg. No. 47,671

Fish & Richardson P.C.
12390 El Camino Real
San Diego, California 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10374241.doc

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV399289561US

March 9, 2004

Date of Deposit

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-913001	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Bratin Saha	
		Filing Date March 9, 2004	Group Art Unit

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	5,428,807	06/27/1995	McKeen et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						

Foreign Patent Documents or Published Foreign Patent Applications							
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
	AH						
	AI						
	AJ						
	AK						
	AL						

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AM	Dean M. Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism", Proceedings of the 22 nd Annual International Symposium on Computer Architecture, Santa Margherita Ligure, Italy, June 1995
	AN	Professor Bill Dally, "Beyond Instruction Level Parallelism – Multithreading", EE482: Advanced Computer Organization, Processor Architecture, Lecture #12, Stanford University, May 8, 2000
	AO	Glenn Hinton et al., "The Microarchitecture of the Pentium® 4 Processor", Intel Technology Journal 1 st quarter 2001, http://developer.intel.com/technology/itj/q12001/articles/art_2a.htm
	AP	Jeffrey Oplinger et al., "Enhancing Software Reliability with Speculative Threads", ACM 1-58113-574-2/02/0010, 2002
	AQ	Haitham Akkary et al., "A Dynamic Multithreading Processor", Microcomputer Research Labs, Intel Corporation; Department of Electrical and Computer Engineering, Portland State University

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	